Through Silicon Vias cleaning for quantum computer interconnects integration

Harold LE TULZO[1], Loriana CELESTE[1], Jaber DERAKHSHANDEH[2], Carine GERETS[2], Jean CHARBONNIER[3], Candice THOMAS[3], Edouard DESCHASEAUX[3], Jérôme DAVIOT[1]

[1] *Technic France, 15 rue de la Montjoie, BP 79, 93212 Saint-Denis La Plaine, France*
[2] *IMEC, Kapeldreef 75, 3001 Leuven, Belgium*
[3] *CEA-LETI, Univ. Grenoble Alpes, F-38000 Grenoble, France*

Quantum computing based on superconducting Josephson junction qubits is an attractive technology path for performing ultra-fast and efficient calculations. The MATQu (**MAT**erials for **Qu**antum Computing) project aims at developing state-of-the-art qubits and is supported by European academic partners, leading Research Technology Organisations (RTO's), and participants in the semiconductor value chain including equipment and chemical suppliers as well as end-users.

Technic France, owing to its expertise in electroplating and surface preparation (stripping, etching, cleaning) has been challenged within the "3D integration and packaging" workflow alongside expert teams from IMEC and CEA Leti. The common goal is to develop and validate a novel interposer design to interconnect in a 3D multi-stacking manner, qubits with readout wafer (see Figure 1) [1].

New materials stacks [2] that are compatible for cryogenic conditions must be integrated for under bump metallization (UBM), solder bumps [3] and through-silicon vias (TSV's). The design of 5 µm diameter TSV with high-quality material bottom-up plating will require efficient surface preparation and complete removal of chemically resilient post etch residues. In the frame of the MATQu project, IMEC and CEA Leti have been focused upon TSV etching and wafer patterning, while Technic France has been focused on TSV cleaning.

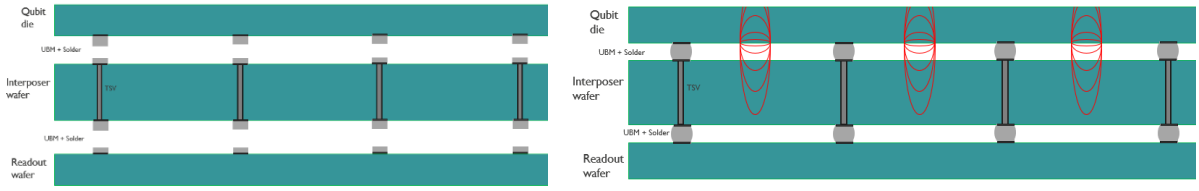

Figure 1 – Solder bumps and TSV formation in interposer wafer for qubit and readout wafers interconnection, before (left) and after (right) bonding.

Following standard Bosch dry etch, high aspect ratio TSV sidewalls are covered with thick inert fluoropolymer, which is detrimental and can cause, among other issues, barrier layer delamination, and an increased thermal stress due to poor fluoropolymer conformality. For quantum applications, this could create loss mechanisms that can damage the coherence and Q factor of qubits, thus reducing device yield [4;5]. Complete removal of these fluoropolymer residues is therefore mandatory.

Current processes of record are either dry (O_2 ashing) or wet [6;7]. Among the wet cleaning solutions, to our best knowledge, none are capable of complete sidewall fluoropolymer and photoresist removal while i) remaining chemically compatible with exposed materials,

especially metals; ii) maintaining a long effective bath life; and iii) avoiding the use of chemical components that are not bioaccumulative nor CMR-listed.

Against these requirements, we have developed TechniClean BOS-347, which has been extensively investigated with partners over several structures patterned by using a standard Bosch dry etch. A comprehensive data set including SEM images, thin-film metrology, and surface analyses such as ToF-SIMS validating post-Bosch etch cleaning efficiency and benchmarking new versus legacy cleaning candidates (wet and ash/wet) will be presented (see Figure 2).

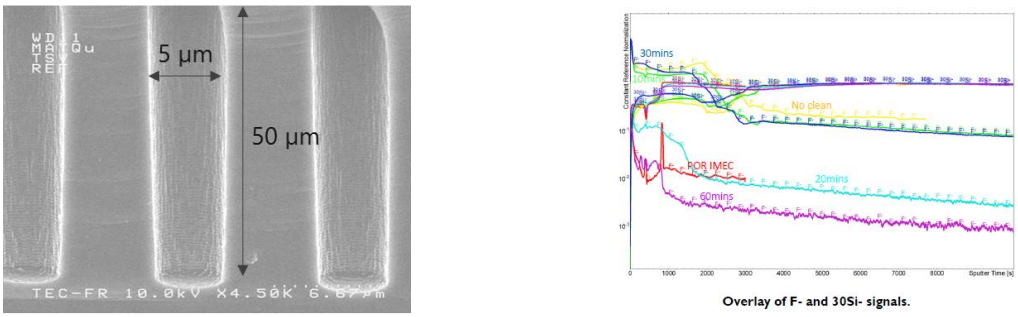

Figure 2 – TSV etched in the frame of the MATQu project by IMEC (left) and ToF-SIMS analyses of the middle parts of the TSV comparing various solutions and processes.

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